400-Mb/s QPSK Repeater for 20-GHz Digital Radio-Relay System

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Abstract—**This paper describes the design and performance of a repeater for a 20-GHz high-speed digital radio-relay system with a transmission capacity of 400 Mb/s. The repeater is totally solid state for miniaturization, high reliability and economy with the adoption of microwave IC's, monolithic IC's, and direct oscillation by Gunn diodes in the 20-GHz band. The modulation and demodulation techniques of the repeater employ QPSK, which has a theoretical advantage over FSK, DPSK, or ASK in error rate performance, considering spectrum utilization. The error rate performance is further improved by using a simple digital equalization for intersymbol interference. The error rate performance of this system was measured. From the test results, it became evident that the equivalent carrier-to-noise ratio (C/N) degradation of error rate performance at a 10^{-6} error rate was about 5 dB under fixed temperature conditions and that the equivalent C/N degradation due to a $-$ 10°C to $+$ 45°C temperature variation was only 1 dB. The experimental 13-hop system employing the repeaters has been operating stably since April 1973.**

I. INTRODUCTION

LARGE capacity transmission systems will be required to meet the growing traffic demand for telephone and various new services, such as video telephone and digital data transmission to be introduced in the near future. However, the common carrier bands below 15 GHz have already been utilized extensively in Japan. It cannot meet the future large traffic demand. The use of higher frequencies has been suggested as a means for meeting the ever increasing demands for communication capacity. Hence, the 20-GHz 400-Mb/s digital radio-relay system is being developed by NTT's Electrical Communication Laboratories.

If the outage time rate of a 2500-km hypothetical reference circuit must be under 0.1 percent per year, rain attenuation at a 20-GHz band forces close repeater spacing which is about 3 km in Japan [1]–[3]. In a system whose repeater spacing is about 3 km, it is necessary to consider cost economy and appearance in designing the repeater station. Therefore, the repeater tower is a self-supporting steel pipe whose standard height is 25 m. Repeater equipment and antennas are mounted on top of the tower. The power supply equipment is located at the bottom of the tower. Because of the increased number of repeaters per system and because the repeaters are mounted on top on the tower, low cost, high reliability, small size, and high capacity repeaters which operate stably in a severe outdoor environment are necessary. Also, a digital modulation technique is needed to reduce the effects of accumulative noise and distortion in the multihop relay system. It was impractical by conventional techniques to satisfy the severe requirements for many repeaters. Therefore, the repeater components, modulation and demodulation techniques, and high-speed pulse transmission techniques have been studied by NTT Laboratories since 1969. Prototype repeaters were manufactured in 1970. After improving the prototype repeaters, the first practical 20-GHz high-speed digital radio repeaters, which are being used for the experimental multihop link (Musashino–Yokosuka, 13 hops) were completed in 1972 [1], [4]. Experimental investigations have shown successful performance and stability. The repeater involved the following new techniques.

1) The repeater has used solid-state circuits in hybrid integrated circuit (HIC) format for miniaturization, high-reliability and economy with the adoption of direct oscillation by Gunn diodes in the 20-GHz band.

2) GaAs Schottky-barrier diodes are used as the switching diodes in a path length switch-type phase modulator in the 20-GHz band.

3) Coherent detection is accomplished by accurate, stable, wide-band intermediate frequency (IF) (1.7 GHz) carrier recovery using a phase-locked loop with a reverse modulator and temperature-compensated delay line.

4) Improvement of the bit error rate performance is implemented by a simple digital intersymbol interference equalizer.

II. REPEATER DESIGN

The specifications and features of the experimental 20-GHz digital radio repeater are shown in Table I. The repeater has a capacity of 400 Mb/s, which is equivalent to 5760 telephone channels, and utilizes quadriphase-shift keying (QPSK) modulation and coherent detection. The choice of 1.7-GHz IF results from a tradeoff between the gain of microwave transistors and the ratio of bandwidth to intermediate center frequency, together with interferences from other systems, such as radars and microwave common carrier systems.

Fig. 1 shows a level and block diagram of the repeater. To ease the problem of transporting a spare repeater to a repeater station and to simplify exchanging the repeater, the repeater packages consist of a digital transmitter, a digital receiver, a digital demodulator, and a dc–dc

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TABLE I
SPECIFICATIONS AND FEATURES OF EXPERIMENTAL 20-GHz DIGITAL RADIO REPEATER

RF band	17.7 to 21.2 GHz
Modulation	QPSK
Demodulation	Coherent detection
Timing frequency (f_p)	About 200 MHz
Bit rate	About 400 Mb/s
Transmitting power	18.5 dBm
Receiver noise figure	11 dB
IF	1700 MHz
Constitution	IC's (converter, IF-band circuits and baseband circuits) Waveguide circuits (RF-band circuits) All solid state
RF power amplifier	Injection-locked oscillator
Equalization	Digital equalizer in time domain
Allowable temperature range	−10°C to 45°C

TABLE II
FILTER BANDWIDTH AND CONSTRUCTION FOR THIS DIGITAL TRANSMISSION SYSTEM

	3-dB Bandwidth (MHz)	Midband Loss (dB)	Construction
Transmitting RF filter	±200	1.0	five-stage maximally flat
Transmitting branching filter	±150	0.25	two-stage maximally flat
Receiving branching filter	±150	0.25	two-stage maximally flat
Receiving RF filter	±600	0.3	four-stage maximally flat
IF filter	±200	1.0	two-stage maximally flat
Low-pass filter	110		five-stage maximally flat time delay

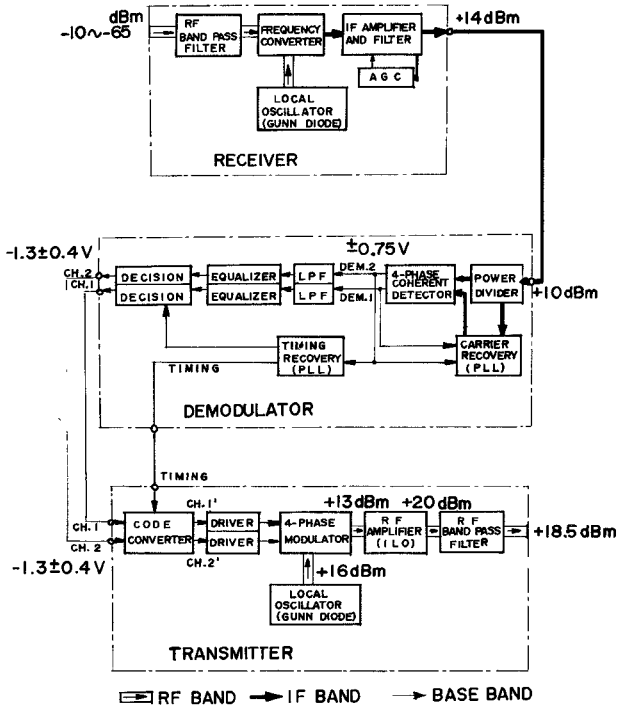


Fig. 1. Level and block diagram of the 20-GHz digital radio repeater.

converter. These units are all designed with the same plug-in form and size (300 × 320 × 80 mm³). To protect hybrid IC's from the environment, they are all airtight with O-rings. In the transmitter, two separate 200-Mb/s input digital signals (CH 1, CH 2) are reshaped and code converted from alternative binary code to natural binary code. The four-phase modulator is driven by the two code-converted digital signals (CH 1′, CH 2′), giving an output modulation rate of 400 Mb/s at a 20-GHz carrier frequency. An injection-locked Gunn amplifier boosts the output to the higher level (+20 dBm) required by the system. In the receiver, the 20-GHz received signal is converted into a 1.7-GHz IF signal by the frequency converter and the IF signal is amplified up to a +14 dBm level which is sufficient for demodulation during fading conditions. The level is maintained by an automatic gain control (AGC) circuit. In the demodulator, a four-phase coherent detector with a carrier recovery circuit using a phase-reverse modulator and a phase-locked loop (PLL) demodulates the receiving IF signal into two 200-Mb/s baseband signals. The digital equalizer compensates for the intersymbol interference due to severe band limitation in overall transmission performance. The two compensated demodulation signals are regenerated by the decision unit and regenerator. The two regenerated signals are the demodulator output.

Efficient spectrum utilization is of great importance in any radio system. Thus this radio-relay system utilizes multilevel (four-level) PSK modulation and two orthogonal polarized waves and radio channel frequency spacing of this system is possibly narrowed. Using digital equalizer techniques, the radio channel spacing and the overall transmission frequency band can be narrowed without large degradation of the error rate performance. The overall 3-dB bandwidth of this system was set at $0.7f_p$ ($= \pm 70$ MHz), where f_p is a timing frequency which is 200 MHz in this system. The choice of $0.7f_p$ results from a tradeoff between intersymbol interference due to band limitation and interchannel interference power from both adjacent channels. System filter constructions are indicated in Table II.

The overall performance of the digital radio repeater is evaluated by necessary overall bandwidth, transmitting power, receiver noise figure (NF), and error rate performance. The overall transmission bandwidth determines the total transmitting capacity in the limited radio-frequency (RF) band. The transmitting power, the receiving noise figure, and the error rate performance define a rain attenuation margin to which the repeater spacing is proportional. The specifications of the transmitting power and the NF of the repeater are, respectively, 18.5 dBm and 11 dB, as shown in Table I.

Specifications of the component circuits were decided by the equivalent carrier-to-noise ratio (C/N) degradation of the error rate performance due to circuit degradation. Table III shows the specifications and the equivalent C/N degradation values of the component circuits, where the equivalent C/N degradation means the C/N (dB) difference between the theoretical value without band

TABLE III
ERROR RATE DEGRADATION FACTOR AT ERROR RATE OF 10^{-6}

Degradation Factor	Specification	Equivalent C/N Degradation (dB)		
		Fixed+Variable	Fixed Temp.	Var. Temp.
Intersymbol interference	$B_R T=1.5$ $B_B T=0.95$	2.4	2.4	
Linear delay distortion	$\Delta T_1/T < 0.05$	0.2	0.2	
Quadratic delay distortion	$\Delta T_2/T < 0.2$	0	0	
Linear amplitude distortion	$\Delta A < 0.5$ dB	0.2	0.2	
Echo distortion	$C/N_e \geq 31$ dB	0.2	0.2	
Recovered reference carrier phase error	$\lvert\Delta\theta_c\rvert \leq 5°$	0.6		0.6
Recovered reference carrier jitter	$C/N_c \geq 30$ dB	0.3	0.3	
Modulation phase error	$\lvert\Delta\theta_m\rvert \leq 5°$	0.6		0.6
Decision level variation	$\lvert\Delta V_t/V_0\rvert \leq 0.1$	0.6		0.6
Uncertain region of decision circuit	$T'/T \leq 0.05$	0.2	0.2	
Clock phase error	$\lvert\Delta\theta'_c\rvert \leq 5°$	0.1		0.1
Injection-locked amplifier	$B \geq 800$ MHz	0.8	0.8	
Modulator rise time	$t_r/T \leq 0.2$ ($t_r \leq 1$ns)	0.3	0.3	
Total (dB)		6.5	4.6	1.9

Note: T: $1/f_p$ (f_p: timing frequency); B_B: bandwidth of branching filter; B_R: receiver bandwidth; $\Delta T_1, \Delta T_2$: linear and quadratic delay distortion at $\pm f_p$; ΔA: linear amplitude distortion at $\pm f_p/2$; C: carrier power; N_e: interference power due to echo; $\Delta\theta_c$: recovered carrier phase error; N_c: interference power due to jitter; $\Delta\theta_m$: modulation phase variation; V_t: decision level drift; V_0: amplitude of eye aperture; T': uncertain region of decision circuit; $\Delta\theta'_c$: clock phase error; B: bandwidth of injection-locked amplifier; t_r: modulator rise time.

limitation and the experimental one to achieve the same error rate. As is evident, the total value of the equivalent C/N degradation is 6.5 dB at an error rate of 10^{-6}. The equivalent C/N degradation value is 4.6 dB under fixed temperature conditions and is 1.9 dB over the temperature range -10°C to $+45$°C.

III. REPEATER PERFORMANCE

The performances of the experimental repeater components are now described.

A. Digital Transmitter

As shown in Fig. 1, the digital transmitter is composed of a local oscillator, a code converter, two diode drivers, a four-phase modulator, an RF power amplifier, and an RF bandpass filter. Fig. 2 shows the digital transmitter. It is airtight, with an aluminum cover and an O-ring. The heat sink of the Gunn oscillator, the Gunn RF amplifier, and the diode driver are of aluminum.

1) Local Oscillator: It is necessary for the local oscillator to have a high-frequency stability and no oscillation mode jumping. To satisfy these characteristics, a Gunn diode oscillator using a band reflection cavity is employed [5]. This oscillator consists of a rectangular-waveguide Gunn diode mount, a half-wavelength waveguide section, a high-Q cavity, and a matched dummy load connected in series, as shown in Fig. 3. This oscillator has a single-mode oscillation and high-frequency stability. The realized frequency and output power stability performances of the 20-GHz carrier wave are, respectively, $+2 \sim -3$ MHz and ± 1.2 dB over a temperature variation of from -10°C to $+60$°C. The realized oscillator output power is 19 dBm, which is more than the specification of 16 dBm. Because the maximum handling power of the four-phase modulator is 16 dBm, the output power is adjusted at the 16-dBm fixed level by a variable attenuator.

2) Four-Phase Modulator and Driver: The four-phase modulator should handle the +16 dBm local oscillator output power. The diode driver output amplitude decides the handling power of the modulator. From the experimental results, the output amplitude was decided as follows:

"1" (forward): 36 mA, "0" (reverse): -5 V.

Fig. 4(a) shows the output pulse. As shown in Fig. 4(a), the rise time and the amplitude of the realized driver output are, respectively, 1.0 ns and 5 V. As shown in Fig. 5, the four-phase modulator consists of 0-$\pi/2$ modulator and 0-π modulator connected in series. Both 0-$\pi/2$ and 0-π modulators are path length modulators which consist of circulators, GaAs Schottky-barrier diode switches, and short plungers which alternate the carrier path length by the switches [6].

The vector locus of the four-phase modulated wave during 200-Mb high-speed operation is shown in Fig. 6(a). Fig. 6(a) shows that there are quadrature components [7] at all phase changes, and that a quadrature component at the phase change of from 0 to $3\pi/2$ is the largest. It causes the interference between two four-phase-demodulated signals (DEM 1 and DEM 2, which are shown in Fig. 1). This quadrature component degrades the error rate performance [8]–[10]. The value of the quadrature component of the modulator output signal is proportional to its rise time t_r [9]. Therefore, the rise time should be as fast as possible. The equivalent C/N degradation due to the quadrature component caused by

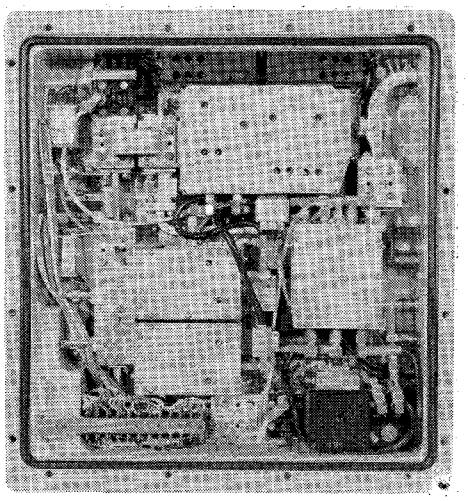


Fig. 2. A 20-GHz digital transmitter. Size (mm): 300 × 320 × 80.

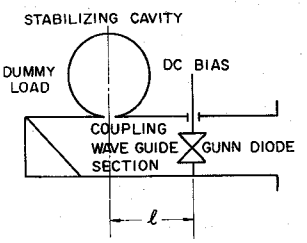


Fig. 3. Arrangement of a band reflection-type frequency stabilized Gunn oscillator.

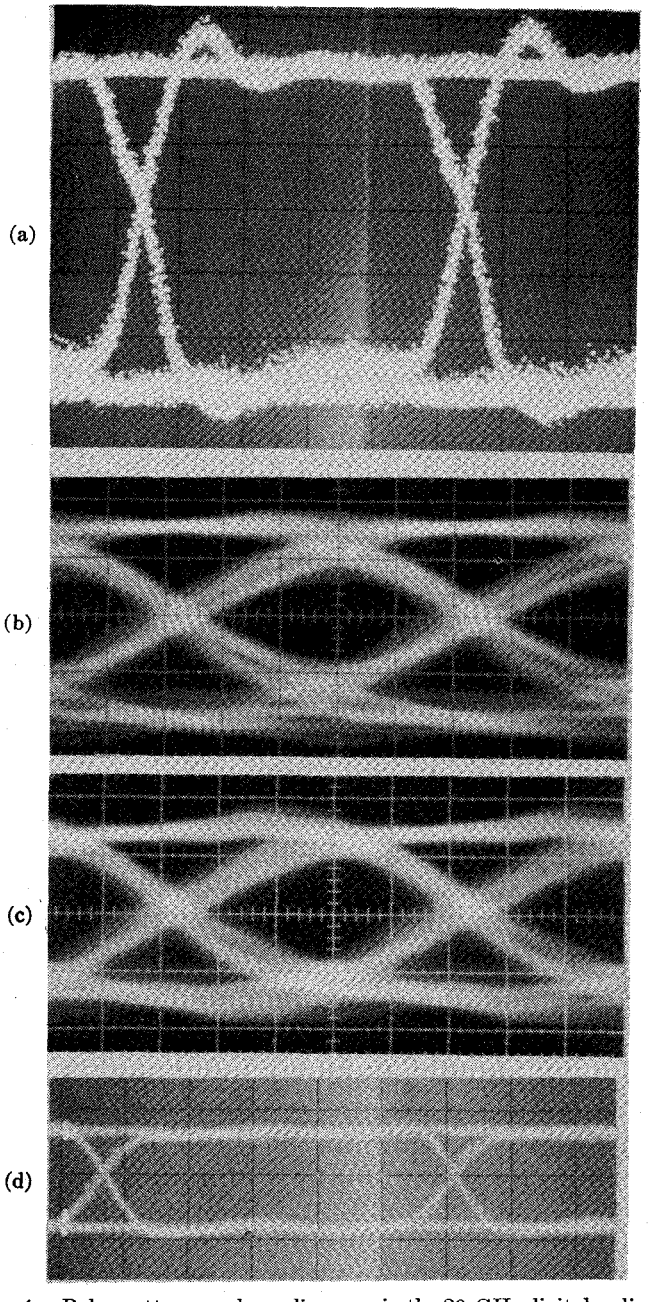


Fig. 4. Pulse patterns and eye diagrams in the 20-GHz digital radio repeater. The transmitting and receiving filters are included in this measurement. Horizontal scale: 1 ns/div. Vertical scale: 1 V/div. (a) Driver output. (b) LPF output. (c) Equalizer output. (d) Regenerator output.

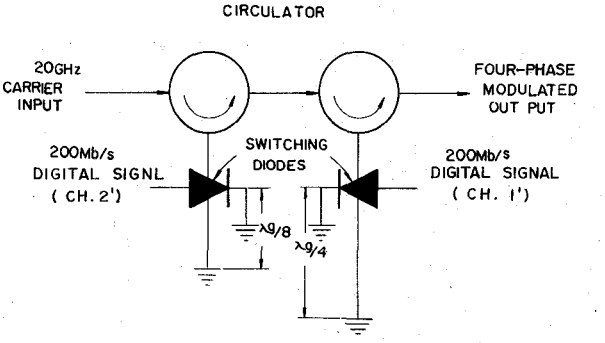
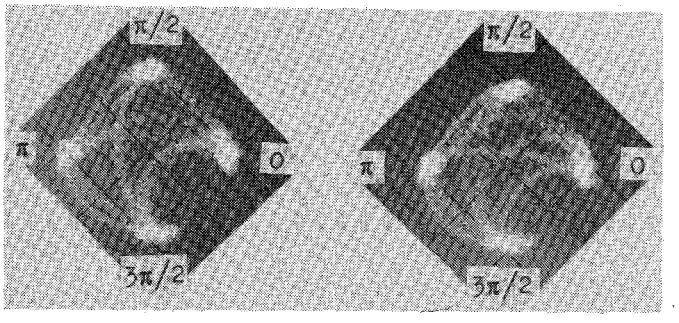


Fig. 5. Four-phase modulator.



(a) (b)

Fig. 6. Vector loci of the four-phase modulated signal. (a) Modulator output. (b) RF amplifier output.

the four-phase modulator was calculated by Saikawa [9] and is 0.3 dB when modulator rise time t_r is $0.2T$ ($T = 1/f_p$). In consideration of the error rate performance degradation, the modulator rise time t_r was decided upon as less than 1.0 ns ($t_r/T = 0.2$).

The loss, maximum modulated phase error, output power, and rise time of the modulator in the experimental repeaters are, respectively, 3.0 dB, 3°, +13 dBm, and 1.0 ns over the temperature range of −10°C to +45°C.

3) RF Amplifier: The experimental four-phase modulator output power of 13 dBm is not sufficient for realizing 3-km repeater spacing. Therefore, this output is amplified by an injection-locked oscillator (ILO) with an output power of more than 20 dBm. The necessary locking bandwidth of ILO is more than ±800 MHz for a gain of 9 dB. So far, there has been no example of RF amplification of the high bit rate modulation signal of 200 Mb using the ILO and little consideration on the effect of the error rate performance. To estimate this effect, the vector locus of the RF amplifier output was measured for the four-phase modulated signal. It is shown in Fig. 6(b). This figure shows that this injection-locked amplifier output has a vector locus dislocation from the idealized locus and increased quadrature components. Thus it is estimated, from consideration of Fig. 6(b), that this RF amplifier degrades the error rate performance. The output power and the locking bandwidth of the manufactured RF amplifier are, respectively, 21.4 dBm and +0.91 to −0.84 GHz for a gain of 9 dB.

4) Digital Transmitter Output: There is a variable attenuator for controlling the output power, the RF transmitting filter, a power monitor, an isolator, and bend waveguides between the RF amplifier and the transmitter output terminal. The RF amplifier output power is attenuated by these circuits whose total loss is about 1.5 dB. The transmitting power is adjusted at the 18.5 dBm specification level by the variable attenuator. The measured VSWR at the transmitter output terminal is less than 1.05 which is less than the specification of 1.2.

B. Digital Receiver

As shown in Fig. 1, the digital receiver is composed of a local oscillator, which is the same type as that of the

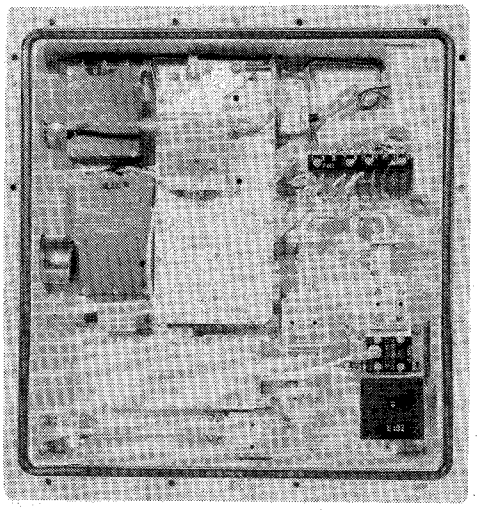


Fig. 7. A 20-GHz digital receiver.

transmitter, RF bandpass filter, frequency converter, preamplifier, and main IF amplifier with an AGC circuit. Fig. 7 shows the digital receiver. Its construction is similar to that of the digital transmitter.

1) Frequency Converter: The frequency converter in the experimental receiver is a balanced type which consists of a microwave IC using quartz substrate. The diode used in this converter is a GaAs Schottky-barrier diode which has a ceramic case. Measured conversion loss is 5.0 dB which is smaller than the objective value of 5.5 dB.

2) IF Amplifier: The IF amplifier consists of a preamplifier, a bandpass filter, an IF isolator, and a main amplifier with AGC circuit. These circuits, except the AGC control unit and the IF isolator, are fabricated on ceramic substrates with microwave IC techniques. The preamplifier consists of a two-stage low-noise transistor amplifier. The noise figure and the gain of the preamplifier in the experimental repeater are, respectively, about 4.8 dB and 16 dB. The main IF amplifier with AGC circuit to maintain a constant signal level for the demodulator is very compact ($50 \times 160 \times 20$ mm^3) and consists of five two-stage transistor amplifiers, four current-controlled p-i-n attenuators and the control unit. The attenuator is a bridged-T circuit with two p-i-n diodes. It has 14-dB maximum attenuation. Each two-stage amplifier including the attenuator is fabricated on a 1 in^2 alumina substrate. To realize desirable characteristics (mainly frequency response) of the multistage amplifier, we adjusted the IC patterns by scraping or pasting conductive adhesive.

The total gain and the output power of the main amplifier in the experimental repeater are, respectively, 72 dB and 14 dBm, and its AGC range is more than 56 dB. The 3-dB bandwidth is ± 200 MHz, which is nearly equal to that of the IF filter consisting of a two-stage maximally flat filter.

3) Overall Receiver Performance: The measured input and output VSWR's, and the measured overall NF of the realized digital receiver are, respectively, 1.13, 1.13, and 10 dB, which are less than specifications of 1.15, 1.20, and 11 dB, respectively.

C. Digital Demodulator

The digital demodulator consists of a four-phase coherent detector with a carrier recovery circuit, a timing recovery circuit, two low-pass filters, two digital equalizers, and two decision units. The digital demodulator is shown in Fig 8.

1) Four-Phase Coherent Detector: Because the demodulation technique of this repeater is coherent detection, the reference carrier must be derived from the incoming signal. There are many carrier extraction techniques, such as the frequency-quadruple method, the baseband-multiplying method and the four-phase reverse-modulation method [11]. Because the same frequency band can be treated, and the S/N of the extracted signal is large, the four-phase reverse-modulation method is employed in this experimental repeater. Fig. 9 shows a four-phase coherent detector with the carrier recovery circuit employed in this repeater [11]. It consists of a four-phase detector, a phase-reverse modulator, and a PLL. It is most important, in assuring stability of a repeater, to make the carrier recovery circuit stable. Therefore, all elements of this circuit are IC structures, which can withstand vibration and temperature variation. Using teflon cable with a positive temperature coefficient in delay time and a ceramic stripline with a negative temperature coefficient as a delay line, the phase error of the reference carrier is made extremely small. For system stability, a wide pull-in range in a PLL is necessary, but the wider the pull-in range is, the worse the S/N of the recovered carrier becomes, in general. In order to make these two contradictory conditions compatible, the automatic voltage-controlled-oscillator (VCO) frequency sweep method [12], [13] is employed in this phase-locked loop. The good S/N of the recovered carrier is realized by narrowing the PLL bandwidth and the wide pull-in range in the narrow-bandwidth PLL is also realized by the automatic VCO frequency sweep method. The frequency sweep is obtained by applying a sweep voltage to the VCO frequency control input, as shown in Fig. 9, and the loop will lock up as the VCO frequency becomes equal to the input frequency. The VCO sweep voltage is driven from an automatic oscillator (1 kHz) which operates only when the loop is unlocked. Its operation depends on the VCO control input impedance difference between the locked state and the unlocked state [13].

Using these techniques, this realized carrier recovery circuit has excellent performance, including: 1) recovered carrier C/N of 32 dB, 2) a pull-in range of ± 10 MHz, and 3) steady phase error of less than 5° over the temperature range of -10°C to $+60$°C. An example of the carrier recovery performance in the experimental repeater is shown in Fig. 10.

The four-phase detector is constructed of two-phase detectors, which consist of branch-line-type hybrid circuits, diode detectors, and dc amplifiers. The measured

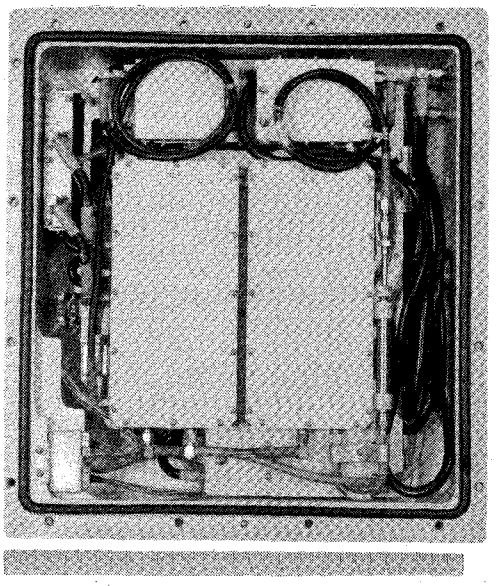


Fig. 8. A 20-GHz digital demodulator.

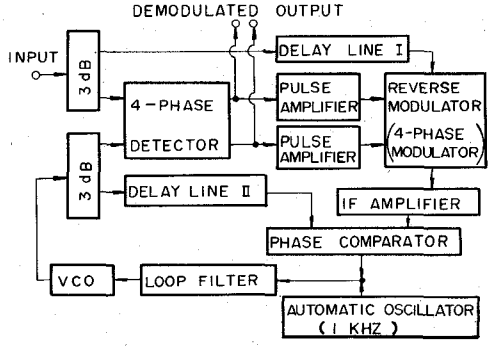


Fig. 9. Block diagram of a four-phase coherent detector with carrier recovery circuit.

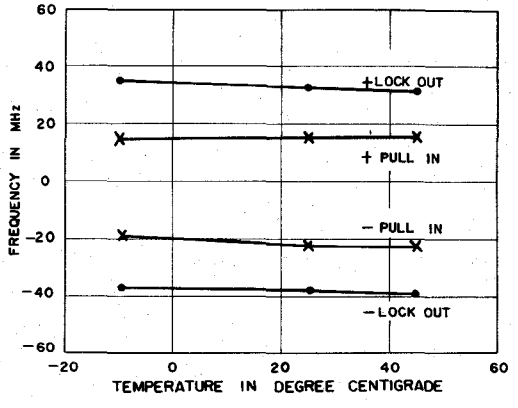


Fig. 10. Carrier recovery performance.

rise time and the measured output voltage of the experimental four-phase detector are, respectively, 1.5 ns and 1.5 V.

2) Low-Pass Filter: A low-pass filter (LPF) can be substituted for an IF bandpass filter for the linear transmission system such as this one. The LPF is adopted for the following reasons in this system. 1) Good carrier recovery performance. 2) Easy manufacture and low cost.

The eye pattern observed at the LPF output is shown in Fig. 4(b).

3) Timing Recovery Circuit: The timing recovery circuit of this repeater consists of a timing extractor, a low-Q resonator, a limiter, and a high-Q PLL. The timing information is extracted from a demodulated nonreturn-to-zero (NRZ) signal by a simple fullwave rectifier consisting of a monolithic logic circuit, as shown in Fig. 11 [14]. The extracted signal is injected into a resonator whose $Q = 20$. Its output level variation due to the pattern variation of the demodulation sequence is limited by the limiter constructed of two monolithic logic circuits. The output of the limiter is injected into the PLL, which acts as a narrow-band timing active filter to reduce timing jitter. Performances of the realized timing recovery circuit are Q of 10 000, pull-in range of 20 kHz, and static phase error of less than 5° over the temperature range of -10°C to $+60$°C. The measured root-mean-square timing jitter due to a random pattern for one repeater is 0.3°.

4) Digital Equalizer and Decision Circuit: In the 20-GHz radio-relay system, a digital equalizer is employed. In this system, the frequency band is narrowed for efficient spectrum utilization. As a result of severe band limitation, a large amount of intersymbol interference appears. Thus a digital equalizer is used to compensate for intersymbol interference in the time domain. Construction of the digital equalizer and the decision circuit is shown in Fig. 12. In this transmission system, whose filter characteristics are shown in Table II, a given pulse will cause intersymbol interference at only the preceding sampling time and not at the next sampling time. Therefore, this digital equalizer cancels only intersymbol interference caused from the next pulse, as shown in Fig. 12 [15].

The eye diagram of equalized signal is shown in Fig. 4(c). The equalizer effect is shown in Fig. 13 as the error

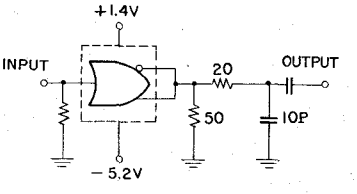


Fig. 11. Timing extractor.

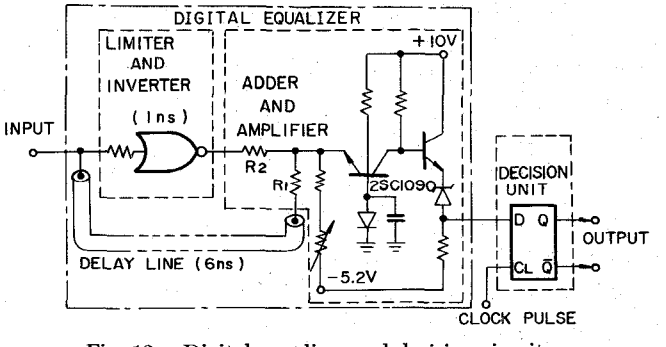


Fig. 12. Digital equalizer and decision circuit.

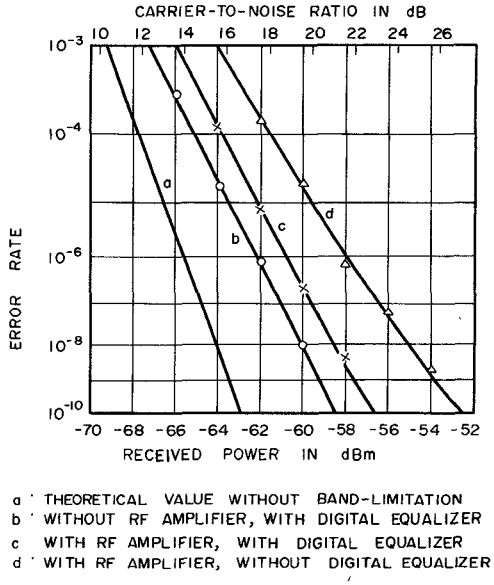


Fig. 13. Error rate performance of the 20-GHz digital repeater (I)

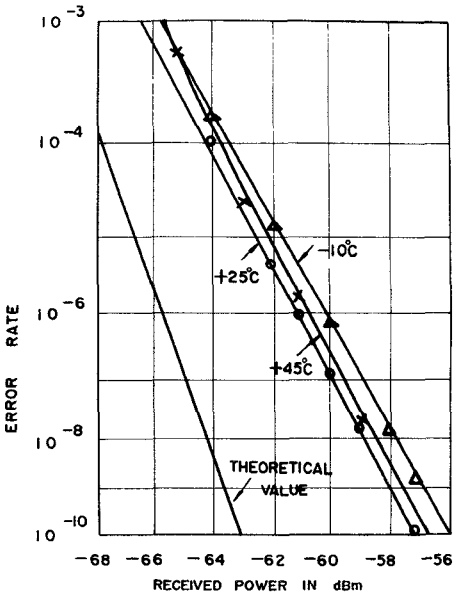


Fig. 14. Error rate performance of the 20-GHz digital repeater (II).

rate performance. As can be seen from Fig. 13, the equivalent C/N improvement obtained by the equalizer is about 3 dB.

The decision circuit employed in this repeater is a D flip-flop monolithic IC which is small in size and low in cost. The eye diagram of the regenerated signal is shown in Fig. 4(d).

IV. OVERALL ERROR RATE PERFORMANCE

In order to evaluate the overall performance of the experimental 20-GHz digital radio-relay system which consists of the 20-GHz digital repeater and branching filters, the overall error rate performances were measured by two 511-bits pseudorandom pulse sequences. Fig. 13 and Fig. 14 illustrate error rate performances under various conditions. Due to employing the coherent detection in this system, there are four error rate curves according to four recovered reference carrier phases. The error rate performances for worst case are shown in Figs. 13 and 14. The four-phase coherent detector with the carrier recovery circuit operates without the error rate degradation over the demodulator input level of +5 dBm to +15 dBm. Therefore, this repeater operates normally over the receiver input level of −70 dBm to −5 dBm.

Fig. 13, which is the measured error rate performance under fixed temperature condition, shows the following.

1) The equivalent C/N degradation due to RF power amplifier is 1.3 dB at an error rate of 10^{-6}, which is larger than the design value. This degradation is caused by increase of quadrature component, as described in Section III-A.

2) The improvement of C/N obtained by the digital equalizer is about 3 dB.

3) The equivalent C/N degradation under fixed temperature conditions is about 5 dB, which is nearly equal to the design value.

As shown in Fig. 14, the equivalent additional C/N degradation due to the ambient temperature variation of −10°C to +45°C is only 1 dB, which is less than the design value of 1.9 dB. Because of designing the component circuits in the repeater to reduce their performance degradation due to temperature variation, stable repeater operation at a wide range of temperature variation was realized. From these tests, it was verified that the overall equivalent C/N degradation of the experimental 20-GHz digital transmission system at the error rate of 10^{-6} is 6 dB, which is less than the 6.5-dB C/N degradation evaluated from specifications of the component circuits in the repeater.

It was also verified that no error rate performance degradation is caused by dc supply voltage variation of from −39 V to −55 V.

V. CONCLUSION

In realizing the 20-GHz digital radio-relay system, decrease of the repeater spacing causes many difficulties such as accumulation of noise and distortion and problems regarding reliability and economy. These difficulties have, however, been overcome by the advance of high-speed multilevel digital modulation and wide-band microwave carrier recovery techniques, solid-state and MIC techniques, and digital equalization. Using these new device and circuit techniques, practical high-speed digital repeaters for this system have been accomplished for the first time anywhere in the world. Experimental test results show that component performances and overall performances of the repeaters are satisfactory and that the repeaters operate stably in spite of temperature and power supply voltage variations. From these test results, it has been verified that the repeaters for 20-GHz digital radio-relay system are suitable for practical use.

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Improved Microwave Repeaters for Hungarian All-Solid-State Communications Systems

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***Abstract*—Improvements in microwave repeaters are outlined utilizing new circuit concepts for the receiver, transmitter, and branching-filter systems. In this way, a 1.5-dB decrease in the receiver noise figure and a 1-dB reduction in the attenuation of branching-filter systems are obtained with a simultaneous 2-dB overall increase of transmitter-multiplier and upconverter efficiencies, resulting in a higher signal-to-noise ratio. An improvement is achieved in the AM-to-PM conversion and group-delay characteristics, too. The new circuits have been developed for Hungarian all-solid-state communications systems operating in the 4-, 6-, and 8-GHz frequency bands.**

I. INTRODUCTION

IMPROVEMENTS in microwave repeaters are outlined utilizing new circuit concepts for the receiver, transmitter, and branching-filter systems. In this way, an essential reduction in the receiver noise figure and in the attenuation of branching-filter systems is obtained with a simultaneous increase of transmitter-multiplier and upconverter efficiencies, resulting in a higher signal-to-noise ratio. The new circuits have been developed for Hungarian all-solid-state communications systems operating in the 4-, 6-, and 8-GHz frequency bands. Thus the paper also gives a report on present state-of-the-art techniques in Hungary.

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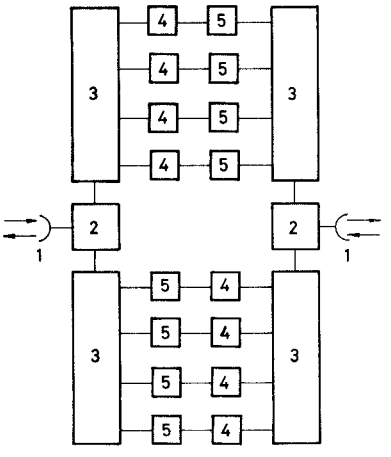

Fig. 1. Schema of a repeater. 1: Antenna. 2: Transmitter–receiver combiner. 3: Branching filter. 4: Receiver. 5: Transmitter.

The schematic of a repeater is shown in Fig. 1. At the repeater stations, one aerial is used in one direction, transmitting four transmitter signals and receiving four receiver signals simultaneously. The transmitter and receiver signals of the same polarization are combined or selected by transmitter–receiver combiners. The transmitter or receiver signals are combined or selected by branching filters.